CLAIMS

What is claimed is:

1. A method of fabricating PMOS and NMOS gate structures in a semiconductor device, the method comprising:

forming a gate dielectric in PMOS and NMOS regions above a semiconductor body;

forming an n-doped first metal silicide above the gate dielectric in the NMOS region;

forming a p-doped first metal silicide above the gate dielectric in the PMOS region;

patterning the first metal silicide in the NMOS and PMOS regions to define NMOS and PMOS gate structures; and

forming a second metal silicide above the doped first metal silicide in the NMOS and PMOS regions.

2. The method of claim 1, wherein the first and second metal silicides are different.

3. The method of claim 1, further comprising forming silicon between the first and second metal silicides in the NMOS and PMOS regions.

4. The method of claim 3, wherein patterning the first metal silicide comprises:

patterning the silicon and the n-doped first metal silicide to form an NMOS gate structure in the NMOS region; and

patterning the silicon and the p-doped first metal silicide to form a PMOS gate structure in the PMOS region.

5. The method of claim 3, wherein forming the second metal silicide comprises:

forming a metal over the silicon; and

reacting the metal with the silicon to create the second metal silicide.

6. The method of claim 5, wherein reacting the metal with the silicon consumes substantially all of the silicon to create the second metal silicide over the doped first metal silicide in the NMOS and PMOS regions.

7. The method of claim 5, wherein the first metal silicide comprises one of molybdenum, tungsten, tantalum, and titanium.

8. The method of claim 5, wherein the second metal silicide comprises nickel.

9. The method of claim 1, wherein the first metal silicide comprises a refractory metal.

10. The method of claim 1, wherein the second metal silicide comprises nickel.

11. The method of claim 1, wherein the first metal silicide comprises one of molybdenum, tungsten, tantalum, and titanium.

12. The method of claim 1, wherein forming the doped first metal silicide above the gate dielectric comprises:

depositing first metal silicide material above the gate dielectric in the NMOS and PMOS regions;

introducing n-type dopants into the first metal silicide material in the NMOS region; and

introducing p-type dopants into the first metal silicide material in the PMOS region.

13. The method of claim 12, wherein introducing n-type dopants into the first metal silicide comprises implanting n-type dopants into the first metal silicide in the NMOS region, and wherein introducing p-type dopants into the first metal silicide comprises implanting p-type dopants into the first metal silicide in the PMOS region.

14. The method of claim 13, further comprising forming silicon over the first metal silicide before implanting n-type dopants into the first metal silicide in the NMOS region and before implanting p-type dopants into the first metal silicide in the PMOS region.

15. The method of claim 12, further comprising forming silicon over the first metal silicide before introducing n-type dopants into the first metal silicide in the NMOS region and before introducing p-type dopants into the first metal silicide in the PMOS region, wherein introducing n-type dopants into the first metal silicide in the NMOS region and introducing p-type dopants into the first metal silicide in the PMOS region comprises:

implanting n-type dopants into the silicon in the NMOS region;

implanting p-type dopants into the silicon in the PMOS region; and

annealing to drive n-type dopants from the silicon into the first metal silicide in the NMOS region and to drive p-type dopants from the silicon into the first metal silicide in the PMOS region.

16. The method of claim 15, wherein patterning the first metal silicide comprises etching the silicon and the first metal silicide in the NMOS and PMOS regions to define NMOS and PMOS gate structures, and wherein forming the conductive gate contacts comprises forming a second metal silicide above the first metal silicide in the NMOS and PMOS regions.

17. The method of claim 12, wherein the first metal silicide comprises one of molybdenum, tungsten, tantalum, and titanium.

18. The method of claim 1, wherein forming the doped first metal silicide above the gate dielectric comprises:

depositing a first metal over the gate dielectric in the NMOS and PMOS regions;

depositing a first silicon over the refractory metal in the NMOS and PMOS regions;

annealing the first metal and the first silicon to form first metal silicide in the NMOS and PMOS regions;

introducing n-type dopants into the first metal silicide in the NMOS region; and

introducing p-type dopants into the first metal silicide in the PMOS region.

19. The method of claim 18, wherein introducing the n and p-type dopants comprises:

depositing a second silicon over the first metal silicide:

implanting n-type dopants into the second silicon in the NMOS region;

implanting p-type dopants into the second silicon in the PMOS region; and

annealing to drive n-type dopants from the second silicon into the first metal silicide in the NMOS region and to drive p-type dopants from the second silicon into the first metal silicide in the PMOS region.

20. The method of claim 19, wherein forming the second metal silicide comprises reacting the second silicon with a second metal above the first metal silicide in the NMOS and PMOS regions.

21. The method of claim 20, wherein reacting the second silicon with the second metal consumes substantially all of the second silicon to create the second metal silicide over the first metal silicide.

22. The method of claim 18, wherein the first metal silicide comprises one of molybdenum, tungsten, tantalum, and titanium.

23. The method of claim 1, wherein forming the doped first metal silicide above the gate dielectric comprises:

depositing a first metal over the gate dielectric in the NMOS and PMOS regions;

depositing a first silicon over the first metal in the NMOS and PMOS regions;

introducing n-type dopants into the first metal in the NMOS region;

introducing p-type dopants into the first metal in the PMOS region; and

annealing the first metal and the first silicon after introducing the n and p-type dopants to form doped first metal silicide in the NMOS and PMOS regions.

24. The method of claim 23, wherein introducing n-type dopants into the first metal comprises implanting n-type dopants through the silicon and into the first metal in the NMOS region, and wherein introducing p-type dopants into the metal comprises implanting p-type dopants through the silicon and into the first metal in the PMOS region.

25. The method of claim 24, wherein the first metal is one of molybdenum, tungsten, tantalum, and titanium.

26. The method of claim 1, wherein forming the doped first metal silicide above the gate dielectric comprises:

depositing a first metal over the gate dielectric in the NMOS and PMOS regions;

depositing a first silicon over the first metal in the NMOS and PMOS regions;

introducing n-type dopants into the first silicon in the NMOS region;

introducing p-type dopants into the first silicon in the PMOS region; and

annealing the first metal and the first silicon after introducing the n and p-type dopants to form doped first metal silicide in the NMOS and PMOS regions.

27. The method of claim 26, wherein introducing n-type dopants into the first silicon comprises implanting n-type dopants into the first silicon in the NMOS region, and wherein introducing p-type dopants into the first silicon comprises implanting p-type dopants into the first silicon in the PMOS region.

28. The method of claim 27, wherein the first metal is a refractory metal.

29. A semiconductor device, comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a gate dielectric above a semiconductor body, an n-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the n-doped first metal silicide; and

a PMOS transistor gate structure, the PMOS gate structure comprising a gate dielectric above a semiconductor body, a p-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the p-doped first metal silicide.

30. The device of claim 29, wherein the first metal silicide comprises a refractory metal.

31. The device of claim 30, wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium.

32. The device of claim 29, wherein the second metal silicide comprises nickel.

33. The device of claim 29, further comprising silicon between the first and second metal silicides in the NMOS and PMOS gate structures.

34. The device of claim 29, wherein the first and second metal silicides are different.

35. A transistor gate structure, comprising:

a gate dielectric formed above a semiconductor body;

a first metal silicide above the gate dielectric, the first metal silicide being doped with n or p-type impurities; and

a second metal silicide above the first metal silicide.

36. The gate structure of claim 35, wherein the first and second metal silicides are different.

37. The gate structure of claim 36, further comprising silicon between the first and second metal silicides.

38. The gate structure of claim 35, wherein the first metal silicide comprises a refractory metal.

39. The gate structure of claim 38, wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium.

40. The gate structure of claim 38, wherein the second metal silicide comprises nickel.

41. The gate structure of claim 35, wherein the second metal silicide comprises nickel.